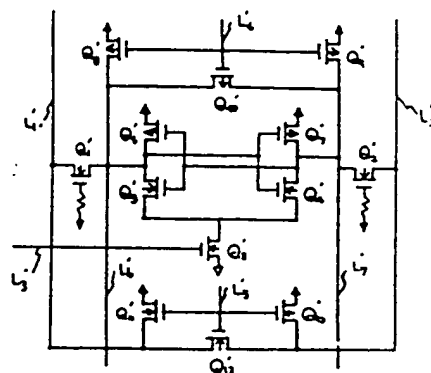


(54) SENSE AMPLIFYING CIRCUIT OF SEMICONDUCTOR STORAGE DEVICE

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PURPOSE: To raise a high speed property in a signal leading-in part, to reduce a current consumption required for pre-charge of a data line, and to shorten a pre-charge time by using an N channel type MOS transistor for the signal leading-in part extending from the data line to a flip-flop circuit.

CONSTITUTION: A timing signal line L'_1 is set to low voltage, an N channel type MOS transistor Q'_5 is set to an off-state, a timing signal line L'_2 is set to low voltage, P channel type MOS transistors Q'_6 , Q'_7 , and Q'_{10} are set to an on-state, and sense input/output lines L'_4 , L'_7 are pre-charged to a supply power source V_{DD} . At the same time, a timing signal line L'_3 is set to high voltage, N channel type MOS transistors Q'_{11} , Q'_{12} and Q'_{13} are set to an on-state, and data lines L'_1 , L'_2 are pre-charged to the potential which has been lowered by a threshold voltage portion of the N channel type MOS transistor from the V_{DD} level. In this case, N channel type MOS transistors Q'_1 , Q'_2 operate as a level shifting element for a voltage drop, and as for the L'_4 , L'_7 , its potential is not drawn by the L'_1 , L'_2 , and they are pre-charged to the V_{DD} level.



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⑭ 半導体記憶装置のセンスアンプ回路

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明 細 書

発明の名称

半導体記憶装置のセンスアンプ回路

特許請求の範囲

(1) 第1, 第2, 第3, 第4のPチャネル型MOSトランジスタのソース電極と、第1, 第2のNチャネル型MOSトランジスタのゲート電極と、第3, 第4のNチャネル型MOSトランジスタのドレイン電極を供給電源に接続し、前記第1および第3のNチャネル型MOSトランジスタのソース電極と、第5のNチャネル型MOSトランジスタのソースまたはドレイン電極とを第1のデータ線に接続し、前記第2および第4のNチャネル型MOSトランジスタのソース電極と、前記第5のNチャネル型MOSトランジスタのドレインまたはソース電極とを第2のデータ線に接続し、前記第1および第3のPチャネル型MOSトランジスタのドレイン電極と、第5のPチャネル型MOSトランジスタのソースまたはドレイン電極と、第

6および前記第1のNチャネル型MOSトランジスタのドレイン電極と、前記第2のPチャネル型MOSトランジスタのゲート電極と、第7のNチャネル型MOSトランジスタのゲート電極とを第1のセンス入出力線に接続し、前記第2および第4のPチャネル型MOSトランジスタのドレイン電極と、前記第5のPチャネル型MOSトランジスタのドレインまたはソース電極と、前記第2および第7のNチャネル型MOSトランジスタのドレイン電極と、前記第1のPチャネル型MOSトランジスタのゲート電極と、前記第6のNチャネル型MOSトランジスタのゲート電極とを第2のセンス入出力線に接続し、前記第6および第7のNチャネル型MOSトランジスタのソース電極と、第8のNチャネル型MOSトランジスタのドレイン電極を接続し、前記第8のNチャネル型MOSトランジスタのソース電極を接地電源に接続し、前記第3, 第4, 第5のPチャネル型MOSトランジスタのゲート電極を第1のプリチャージ信号線に接続し、前記第3, 第4, 第5のNチャネル

型MOSトランジスタのゲート電極を第2のブリチャージ信号線に接続し、前記第8のNチャネル型MOSトランジスタのゲート電極をタイミング信号線に接続して成ることを特徴とする半導体記憶装置のセンスアンプ回路。

(2) 前記第1, 第2, 第3, 第4, 第5のPチャネル型MOSトランジスタをNチャネル型MOSトランジスタにし、かつ前記第1, 第2, 第3, 第4, 第5, 第6, 第7, 第8のNチャネル型MOSトランジスタをPチャネル型MOSトランジスタにし、かつ供給電源と接地電源を入れ替えることを特徴とする前記特許請求の範囲第1項記載の半導体記憶装置のセンスアンプ回路。

発明の詳細な説明

本発明は半導体記憶装置のデータ線に読み出された読み出し出力を検出するためのセンスアンプ回路に関するものである。

従来のセンスアンプ回路例を第1図に示す。 Q_1 , Q_2 はPチャネル型MOSトランジスタ、 Q_3 ,

Q_4 はNチャネル型MOSトランジスタであり、 Q_1 , Q_2 のPチャネル型MOSトランジスタとでフリップフロップ回路を構成しており、 Q_3 , Q_4 のソース電極は共通接続され、Nチャネル型MOSトランジスタ Q_3 を介して接地電源 V_{SS} に接続されており、 Q_1 , Q_2 , Q_3 はPチャネル型MOSトランジスタで、フリップフロップ回路の入出力側のブリチャージのために用意されており、 Q_{11} , Q_{12} , Q_{13} はPチャネル型MOSトランジスタで、データ線のブリチャージのために用意されている。 L_1 はデータ線、 L_2 は L_1 とは補元関係にあるデータ線、 L_3 , L_4 , L_5 はタイミング信号線、 L_6 はセンス入出力線、 L_7 は L_6 とは補元関係にあるセンス入出力線である。

従来の回路の動作を説明する。タイミング信号線 L_5 をハイ電圧とし、Pチャネル型MOSトランジスタ Q_1 , Q_2 をオフ状態にさせ、タイミング信号線 L_6 をロー電圧とし、Pチャネル型MOSトランジスタ Q_{11} , Q_{12} , Q_{13} をオン状態にさせることにより、データ線 L_1 , L_2 がブリチャ

ージされ、同時にタイミング信号線 L_4 をロー電圧とし、Pチャネル型MOSトランジスタ Q_3 , Q_4 , Q_{11} をオン状態にさせることにより、センス入出力線 L_6 , L_7 がブリチャージされる。ブリチャージ時に L_1 をロー電圧とし、 Q_1 , Q_2 をオン状態にさせ、同時にNチャネル型MOSトランジスタ Q_3 をオフ状態にさせ、フリップフロップ回路を不動作状態にさせる。ブリチャージが終了された状態で、 L_1 , L_2 に情報が出力されその情報が Q_1 , Q_2 を通して、センス入出力線 L_6 , L_7 に引き入れられる。 L_6 , L_7 に十分な電位差が生じたところで、 L_5 をハイ電圧とし、 Q_1 , Q_2 をオフ状態にさせ、 Q_3 をオン状態にさせ、フリップフロップ回路が動作して情報の増幅を行ない、増幅された情報が L_6 , L_7 に出力される。

上記のような従来の回路においては、データ線からフリップフロップ回路への信号導入部のPチャネル型MOSトランジスタにタイミング信号線が必要とする。信号導入部にPチャネル型MOS

トランジスタを用いており、信号導入部での信号の伝搬が遅い、またトランジスタサイズが大きくなる。データ線をPチャネル型MOSトランジスタでブリチャージしているために、ブリチャージ電圧が供給電源 V_{DD} レベルまで上がり、このためデータ線を十分ブリチャージするためには時間がかかる、また消費電流が大きいという欠点があった。

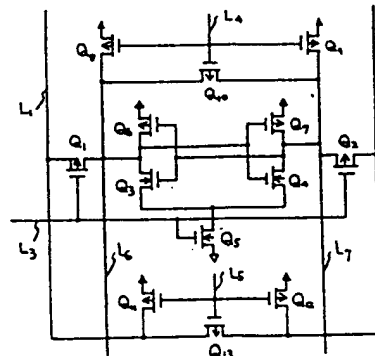
本発明は上記実情を鑑み、この問題を解決すべくなされたもので、その目的はデータ線からフリップフロップ回路への信号導入部でのタイミング信号線の除去と、信号導入部での高速度性を高めデータ線のブリチャージに要する消費電流を小さくし、ブリチャージ時間を短くすることである。

以下図面を参照して本発明の実施例を説明する。第2図は本発明の実施例であり、 L'_1 はデータ線、 L'_2 は L'_1 と補元関係にあるデータ線で、Nチャネル型MOSトランジスタ Q'_1 , Q'_2 を介して、 L'_7 のセンス入出力線に接続されている。で L'_6 , L'_7 は補元関係にある。 Q'_1 , Q'_2 の

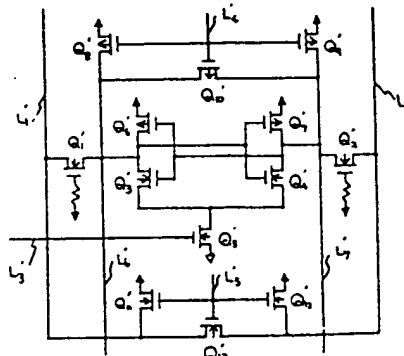
$L'_1, L'_2, L'_3 \dots$ タイミング信号線 $L_4,$
 $L_7, L'_8, L'_7 \dots$ センス入出力線 $Q_1, Q_2,$
 $Q_3, Q_7, Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13}, Q'_1,$
 $Q'_7, Q'_8, Q'_9, Q'_{10} \dots$ Pチャネル型MOSトランジスタ $Q_3, Q_4, Q_5, Q'_1, Q'_2, Q'_3, Q'_4,$
 $Q'_5, Q'_{11}, Q'_{12}, Q'_{13} \dots$ Nチャネル型MOSトランジスタ。
 $\rightarrow VDD$
 $\rightarrow VSS$

以 上

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第 1 図



第 2 図

(Translation)

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(54) Sense-amplifying Circuit for Semiconductor Memory Device

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Specifications

Name of invention: Sense-amplifying Circuit for Semiconductor
Memory Device

Scope of Patent Application: (1) A sense-amplifying current of
a semiconductor memory device characterized by --

- connecting to the power supply the source electrodes of MOS transistors of the 1st, 2nd, 3rd and 4th channel types, gate electrodes of a 1st and 2nd N-channel type MOS transistors and drain electrodes of 3rd and 4th N-channel type MOS transistors;
- connecting to the primary data line source electrodes of the above-noted 1st and 3rd N-channel type MOS transistors, and to the source or drain electrode of an MOS transistor of the 5th N-channel type;
- connecting to the secondary data line the source electrodes of the above-noted 2nd and 4th N channel type MOS transistors and the drain or source electrodes of the above-noted 5th N-channel type MOS transistor
- connecting to the primary sense input/output line the drain electrodes of 1st and 3rd P-channel type MOS transistors, the source or drain electrodes of a 5th P-channel type MOS transistor, the drain electrodes of the 6th and above-noted 1st N-channel type MOS transistors, the gate electrode of the above-noted 2nd P-channel type MOS transistor, and the gate electrode of the 7th N-channel type MOS transistor;
- connecting to the secondary sense input/output line the drain electrodes of the above-noted 2nd and 4th P-channel type MOS transistors, the drain or source electrode of the above-noted 5th P-channel type MOS transistor, drain electrodes of the above 2nd and 7th N-channel type MOS transistors, the gate electrode of the above-noted 1st P-channel type MOS transistor, and the gate electrode of the above-noted 6th N-channel type MOS transistor
- connecting the source electrodes of the above-noted 6th and 7th N-channel type MOS transistors and the drain electrode of an MOS transistor of the 8th N-channel type;
- connecting to the grounding electrode a source electrode of the above-noted 8th N-channel type MOS transistor;
- connecting to the primary precharge signal line the gate electrodes of the above-noted 3rd, 4th and 5th P-channel type MOS transistors;
- connecting to the secondary precharge signal line the gate electrodes of the above-noted 3rd, 4th and 5th N-channel type MOS transistors: and
- connecting to the timing signal line the gate electrode of an MOS transistor of the above-noted 8th N-channel type.*

(2) A sense-amplifier circuit of the semiconductor memory device described in Scope of Patent Application Item 1, characterized by making the above-noted 1st, 2nd, 3rd, 4th and 5th P-channel type MOS transistors into an N-channel type MOS transistor, and also making the above-noted 1st, 2nd, 3rd, 4th, 5th, 6th, 7th and 8th N-channel type MOS transistor into a P-channel type MOS transistor, as well as interchanging the ground power source and the power supply.

*(Translator's note: I formatted the above (1) with dashes to facilitate reading and comprehension. Also, Japanese lacks plural verb and noun forms, so that one must guess singular/plural from the context.)

Detailed Explanation of Invention

This invention bears on a sense-amplifier circuit for detecting reading output read by a semiconductor memory device data line.

Figure 1 shows an example of the usual sense-amplifier circuit. Q_1 and Q_2 are P-channel type MOS transistors; and Q_3 and Q_4 are N-channel type MOS transistors, while the P-channel type MOS transistors of Q_6 and Q_7 make up the flip-flop circuit. The source electrodes of Q_3 and Q_4 are connected in common and tie into ground power source V_{SS} via N-channel type MOS transistor Q_5 . Q_8 , Q_9 and Q_{10} are P-channel type MOS transistors and are provided for precharging the input-output line of the flop-flop circuit. Q_{11} , Q_{12} and Q_{13} are P-channel type MOS transistors provided for precharging the data line. L_1 is a data line, and L_2 is a data line with a supplementary relationship to L_1 . L_3 , L_4 and L_5 are timing signal lines; L_6 is a sense input-output line; and L_7 is an input-output line with a supplementary relationship to L_6 .

I will explain the operation of the usual circuits. By making timing-signal line L_3 high voltage, putting P-channel type MOS transistors Q_1 and Q_2 in an off state, making timing signal line L_5 low voltage and putting P-channel type MOS transistors Q_{11} , Q_{12} and Q_{13} in an on state, data lines L_1 and L_2 are precharged. At the same time, by making timing signal line L_4 low voltage and putting P-channel type MOS transistors Q_8 , Q_9 and Q_{10} in an on state, sense input-output lines L_6 and L_7 are precharged. Making L_3 low voltage while precharged, putting Q_1 and Q_2 in an on state and concurrently putting N-channel type MOS transistor Q_5 in an off state makes the flip-flop circuit go into an inactive state. In a condition where the precharge is ended, data is output to L_1 and L_2 and that data goes through Q_1 and Q_2 to sense input-output lines L_6 and L_7 . When a sufficient voltage difference develops in L_6 and L_7 , L_3 is made high voltage, Q_1 and Q_2 are put in an off state, Q_5 is put in an on state, and the flip-flop circuit operates, does data amplification and amplified data are output to L_6 and L_7 .

In the above-noted usual kind of circuit, timing-signal lines are needed in P-channel type MOS transistors of the signal induction section from the data line to the flip-flop circuit. In the signal induction section a P-channel type MOS transistor is used, signal propagation in the signal induction section is slow, and the transistor becomes larger. Since the data line is precharged by a P-channel type MOS transistor, the precharge voltage rises to the level of the power supply V_{DD} . Therefore, it has the defects that it takes time to sufficiently precharge the data line and current consumption is high.

Given the above situation, this invention is made to resolve such problems; and its goals are to eliminate the timing signal line of the signal induction section from data line to flip-flop circuit, increase speed in the signal induction section and reduce current consumption for precharging the data lines and so to

shorten the precharge time.

Below, we explain an example of applying this invention, referring to Figure 2, an applied example of this invention. L'_1 is a data line; and L'_2 is a data line in a supplementary relationship to L'_1 and connects to sense input-output lines L'_6 and L'_7 via N-channel MOS transistors Q'_1 and Q'_2 . Also, L'_6 and L'_7 are in a supplementary relationship. The [word missing from copy] electrode of Q'_1 and Q'_2 is connected to power supply V_{DD} . To detect data differential inputs, the flip-flop circuit consists of N-channel MOS transistors Q'_3 and Q'_4 and P-channel MOS transistors Q'_5 and Q'_6 . Source electrodes of Q'_3 and Q'_4 are connected in common and connect to ground power source V_{SS} via N-channel MOS transistor Q'_5 . Source electrodes of Q'_6 and Q'_7 connect to power supply V_{DD} . Q'_8 , Q'_9 and Q'_{10} are P-channel MOS transistors provided to precharge the sense input-output line. Q'_{11} , Q'_{12} and Q'_{13} are N-channel MOS transistors provided to precharge the data lines. L'_1 , L'_2 and L'_3 are timing signal lines.

We will explain the operation of this invention's application example.* We make timing signal line L'_3 low voltage, put the N-channel MOS transistor Q'_5 in an off state, make timing signal line L'_1 low voltage, put P-channel MOS transistors Q'_8 , Q'_9 and Q'_{10} in an on state, and precharge sense input-output lines L'_6 and L'_7 to the level of the power supply V_{DD} . Concurrently, we make timing signal line L'_3 high voltage, put N-channel MOS transistors Q'_{11} , Q'_{12} and Q'_{13} in an on state. Data lines L'_1 and L'_2 are precharged from the V_{DD} level to a potential under the N-channel MOS transistor's threshold voltage part. At this point, N-channel MOS transistors Q'_1 and Q'_2 operate as level-shift elements due to the voltage drop and L'_6 and L'_7 are precharged to the V_{DD} level without their potential being drawn off by L'_1 and L'_2 . In a condition of the precharge being ended, L'_1 is made high voltage and L'_2 is made low voltage, while Q'_5 , Q'_6 , Q'_{10} , Q'_{11} , Q'_{12} and Q'_{13} are put in an off state. Data is output to L'_6 and L'_7 and this data is drawn into the sense input-output lines via Q'_1 and Q'_2 . When a sufficient potential differential arises in the input-output line, L'_1 is made high voltage, Q'_3 is put in an on state, the flip-flop circuit operates, data amplification is done and the amplified data is output to L'_6 and L'_7 .

Now, this invention is not limited to the above application example, but can also be made up with the P-channel MOS transistors Q'_3 , Q'_4 , Q'_5 , Q'_6 and Q'_{10} as N-channel MOS transistors, just as N-channel MOS transistors Q'_1 , Q'_2 , Q'_3 , Q'_4 , Q'_5 , Q'_{11} , Q'_{12} and Q'_{13} may be P-channel transistors and the circuits of power supply V_{DD} and ground-source V_{SS} may be interchanged.

As is clear from the above description, by using N-channel MOS transistors in the signal induction section from the data lines to the flip-flop circuit, this invention's circuit can speedily

[Translator's note: The above copy sometimes is blurred, making subscript 3, 5, 6 and 9 virtually indistinguishable. So, there may be some errors here.]

transmit data at the signal induction section and can cut transistor size. Since a gate electrode is connected to the power supply, a timing signal line is not needed. Also, the N-channel MOS transistor of this signal induction section operates as a level-shift element due to the voltage lowering; the sense input-output line precharged to the VDD level by P-channel MOS transistors is not drawn to the data line precharged to the potential to which the threshold voltage part of the N-channel MOS transistor has dropped, so that the VDD level can be sustained. Due to this, the sense input-output line can precharge by the P-channel MOS transistors, and the data line can precharge with N-channel MOS transistors. This creates the advantages that the voltage level of the data line precharge is less, current consumption used for data line precharge can be reduced and the precharge time can be shortened.

Again, this invention has superior effectiveness, making it applicable not merely for integrated circuits for memory but also for micro-processors and one-chip micro-computers having memory circuits as one of their parts, or in such applications as integrated circuits for operating liquid-crystal display panels.

Simple Explanation of Figures

Figure 1 is a circuitry chart showing an example of the usual sense-amplifying circuit.

Figure 2 is a circuitry chart showing the application example of this invention.

[Keys]

L_1, L_2, L'_1, L'_2 data lines
 $L_3, L_4, L_5, L'_3, L'_4, L'_5$ timing signal lines
 L_6, L_7, L'_6, L'_7 sense input-output lines
 $Q_1, Q_2, Q_6, Q_7, Q_8, Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13},$
 $Q'_6, Q'_7, Q'_8, Q'_9, Q'_{10}$ P channel MOS transistors
 $Q_3, Q_4, Q_5, Q'_1, Q'_2, Q'_3, Q'_4,$
 $Q'_5, Q'_{11}, Q'_{12}, Q'_{13}$ N-channel MOS transistors
 $\rightarrow V_{DD}$
 $\rightarrow V_{SS}$

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